WE CLAIM:

1. An integrated circuit structure comprising:

a gate oxide layer;

a titanium boronitride barrier layer above at least a portion of the gate oxide layer;

a polysilicon layer above at least a portion of the titanium boronitride layer; and

a conductive layer above at least a portion of the polysilicon layer, wherein the conductive layer has at least some fluorine atoms or ions therein, and wherein the titanium boronitride barrier layer inhibits diffusion of the fluorine atoms or ions from the conductive layer into the gate oxide layer.

2. The integrated circuit structure of Claim 1 wherein the gate oxide layer has a thickness of about 30 angstroms to about 200 angstroms.

3. The integrated circuit structure of Claim 1 wherein the polysilicon layer has a thickness of about 300 angstroms to about 1,500 angstroms.

4. The integrated circuit structure of Claim 1 wherein the titanium boronitride layer has a thickness of about 50 angstroms to about 500 angstroms.

5. The integrated circuit structure of Claim 1 wherein the conductive layer comprises tungsten.

6. The integrated circuit structure of Claim 1 wherein the conductive layer comprises tungsten silicide.

7. The integrated circuit structure of Claim 1 wherein the conductive layer has a thickness of about 200 angstroms to about 4,000 angstroms.

8. The integrated circuit structure of Claim 1 further comprising a semiconductor substrate.

9. The integrated circuit structure of Claim 8 wherein the semiconductor substrate comprises an intrinsically doped monocrystalline silicon wafer.

10. The integrated circuit structure of Claim 8 wherein the semiconductor substrate comprises an operable portion of a transistor array in a memory device.

11. A gate in an integrated circuit comprising:

a dielectric layer;

a polysilicon layer formed over at least a portion of the dielectric layer;

a diffusion barrier layer comprising titanium boronitride formed over at least a portion of the polysilicon layer; and

a conductive layer formed over at least a portion of the diffusion barrier layer, wherein the conductive layer has at least some fluorine atoms or ions therein, and wherein the diffusion barrier layer inhibits diffusion of the fluorine atoms or ions from the conductive layer into the polysilicon layer.

12. The gate of Claim 11 wherein the dielectric layer is a gate oxide layer.

13. The gate of Claim 11 wherein the gate oxide layer has a thickness of about 30 angstroms to about 200 angstroms.

14. The gate of Claim 11 wherein the polysilicon layer has a thickness of about 300 angstroms to about 1,500 angstroms.

15. The gate of Claim 11 wherein the titanium boronitride has a thickness of about 50 angstroms to about 500 angstroms.

16. The gate of Claim 11 wherein the conductive layer comprises tungsten.

17. The gate of Claim 11 wherein the conductive layer comprises tungsten silicide.

18. The gate of Claim 11 wherein the conductive layer has a thickness of about 200 angstroms to about 4,000 angstroms.

19. The gate of Claim 11 further comprising a semiconductor substrate.

20. The gate of Claim 19 wherein the semiconductor substrate comprises an intrinsically doped monocrystalline silicon wafer.

21. The gate of Claim 19 wherein the semiconductor substrate comprises an operable portion of a transistor array in a memory device.

22. The gate of Claim 11 wherein the diffusion barrier layer inhibits the diffusion of the fluorine atoms or ions from the conductive layer into the dielectric layer.

23. A gate electrode comprising:

a dielectric layer;

a diffusion barrier layer comprising titanium boronitride formed over at least a portion of the dielectric layer;

a polysilicon layer formed over at least a portion of the diffusion barrier layer; and

a conductive layer formed over at least a portion of the polysilicon layer, wherein forming the conductive layer incorporates fluorine atoms or ions into the conductive layer, wherein annealing the conductive layer causes at least a portion of the fluorine atoms or ions to diffuse from the conductive layer to the dielectric layer, and wherein the diffusion barrier layer inhibits fluorine diffusion from the conductive layer into the dielectric layer.

24. The gate electrode of Claim 23 wherein the dielectric layer is a gate oxide layer.

25. The gate electrode of Claim 23 wherein the gate oxide layer has a thickness of about 30 angstroms to about 200 angstroms.

26. The gate electrode of Claim 23 wherein the polysilicon layer has a thickness of about 300 angstroms to about 1,500 angstroms.

27. The gate electrode of Claim 23 wherein the titanium boronitride has a thickness of about 50 angstroms to about 500 angstroms.

28. The gate electrode of Claim 23 wherein the conductive layer comprises tungsten.

29. The gate electrode of Claim 23 wherein the conductive layer comprises tungsten silicide.

30. The gate electrode of Claim 23 wherein the conductive layer has a thickness of about 200 angstroms to about 4,000 angstroms.

31. The gate electrode of Claim 23 further comprising a semiconductor substrate.

32. The gate electrode of Claim 31 wherein the semiconductor substrate comprises an intrinsically doped monocrystalline silicon wafer.

33. The gate electrode of Claim 31 wherein the semiconductor substrate comprises an operable portion of a transistor array in a memory device.